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REMARKS

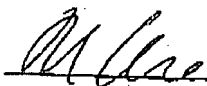
The Office Action of 07/13/2007 has been carefully considered. Reconsideration in view of the present remarks is respectfully requested.

Claims 1-10 were rejected as being inadequately supported in the specification with respect to "a serial memory element in which successive data elements are shifted in order from one memory location to a next successive memory location." Reconsideration is respectfully requested.

Unambiguous support for the foregoing feature is found in Figure 3 of the specification and the accompanying description, page 3, line 33 to page 5, line 16, more particularly page 4, lines 5-8. As can be observed in Figure 3, the serial memory element 32 has successive data elements are shifted in order from one memory location to a next successive memory location (from location 1 to location 2, from location 2 to location 3, etc.). Note the intercoupling of the output of location 1 to the input of location 2, the output of location 2 to the input of location 3, etc. Note also that a common clock signal is applied on line 36 to all of the locations.

Withdrawal of the rejection and allowance of claims 1-10 is respectfully requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: 08/27/2007